

FIG. 1
(PRIOR ART)

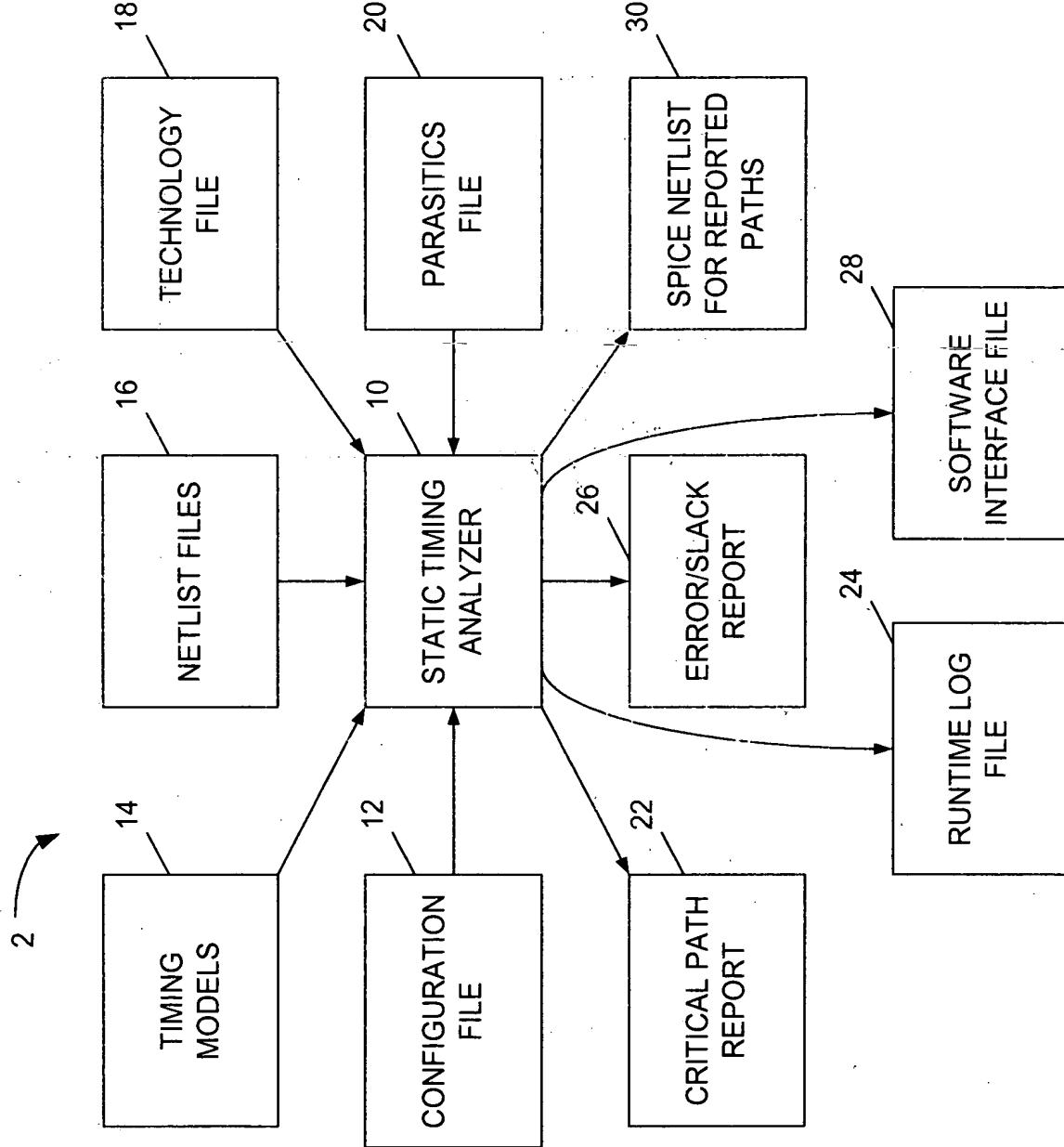


FIG. 2

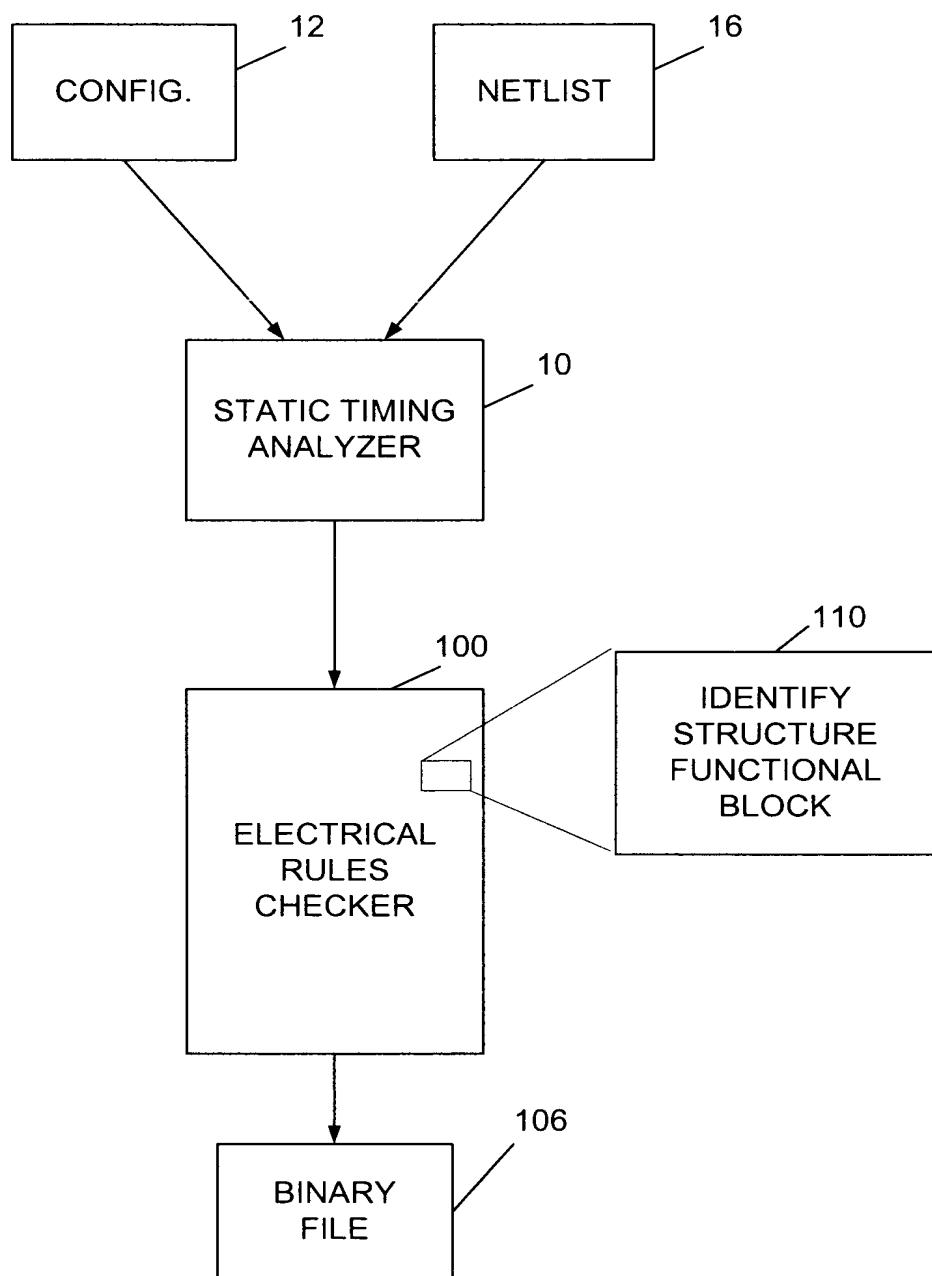


FIG. 3

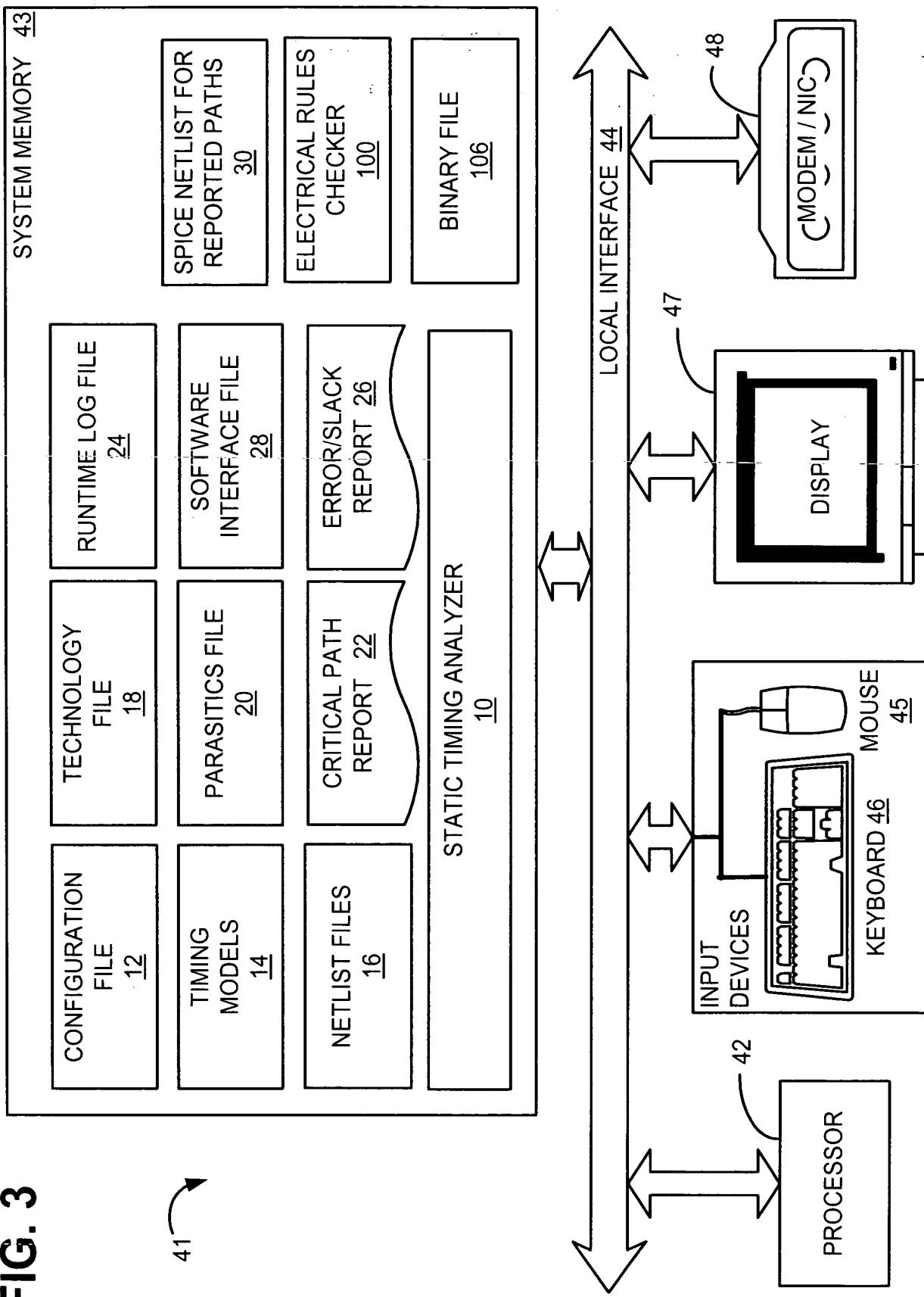


FIG. 4A

ELEMENT {~~~~~

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## Complementary Pass FET

## Special Complementary Pass FET

## RAM Cells

## Single Pass FET

## Feedback FET

## Static Gates

## Probable

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Direction: Unset, Bidirectional, Source-to-Drain, Drain-to-Source,

~~~~~ }

FIG. 4B

NODE {~~~~~

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## Output

## Invert

## Latch

## Precharge

Dynam

## Static

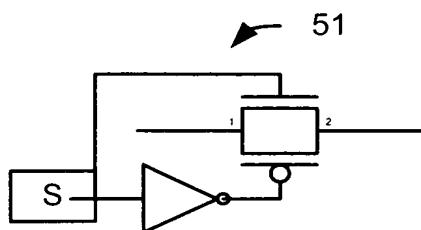
## Clock driver

## Mux Output

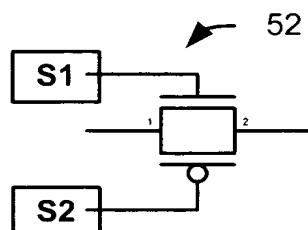
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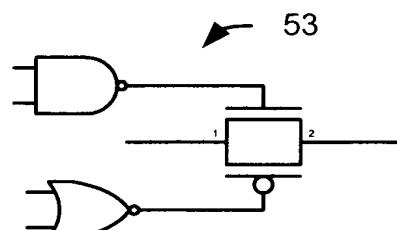
**FIG. 5A**



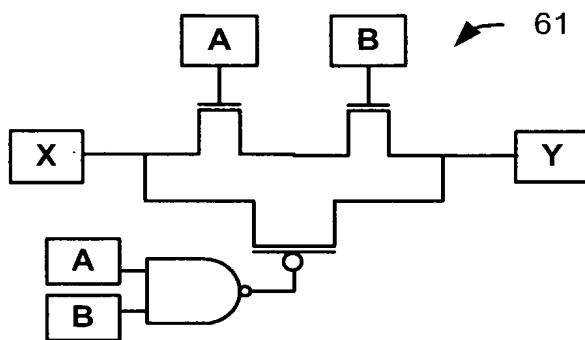
**FIG. 5B**



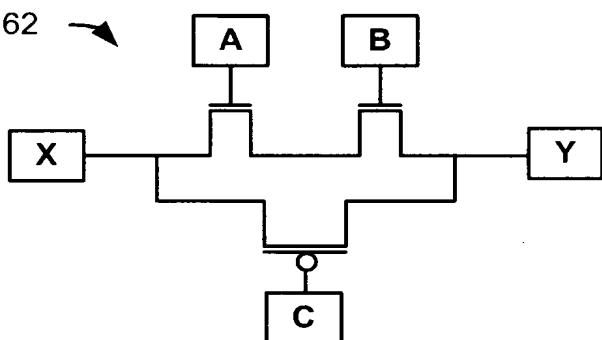
**FIG. 5C**



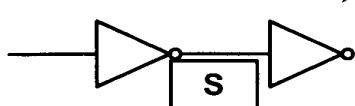
**FIG. 6A**



## FIG. 6B



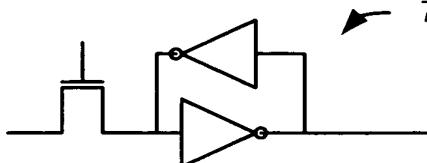
**FIG. 7A**



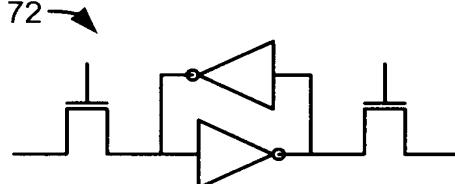
**FIG. 7B**

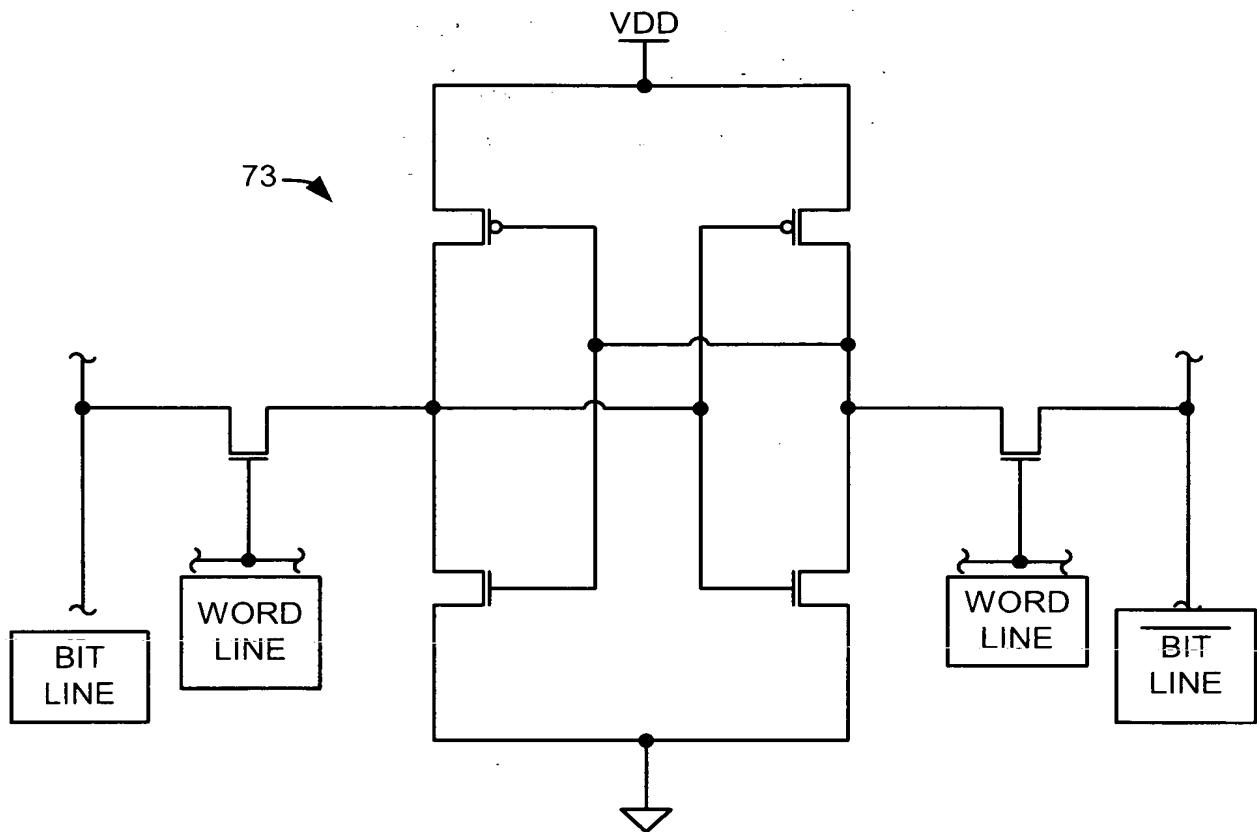


**FIG. 8A**

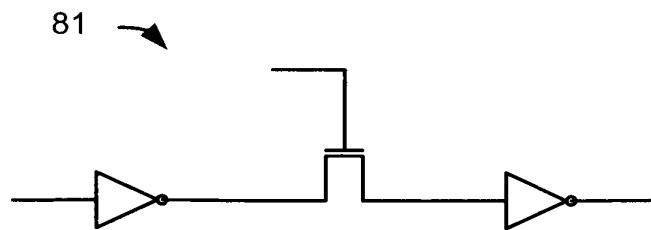


**FIG. 8B**

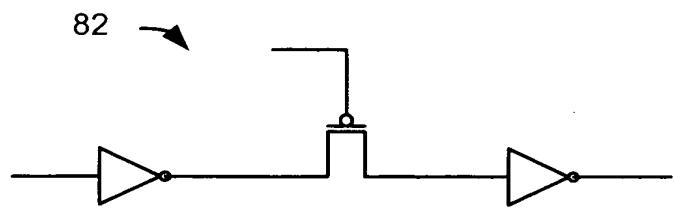




**FIG. 9**



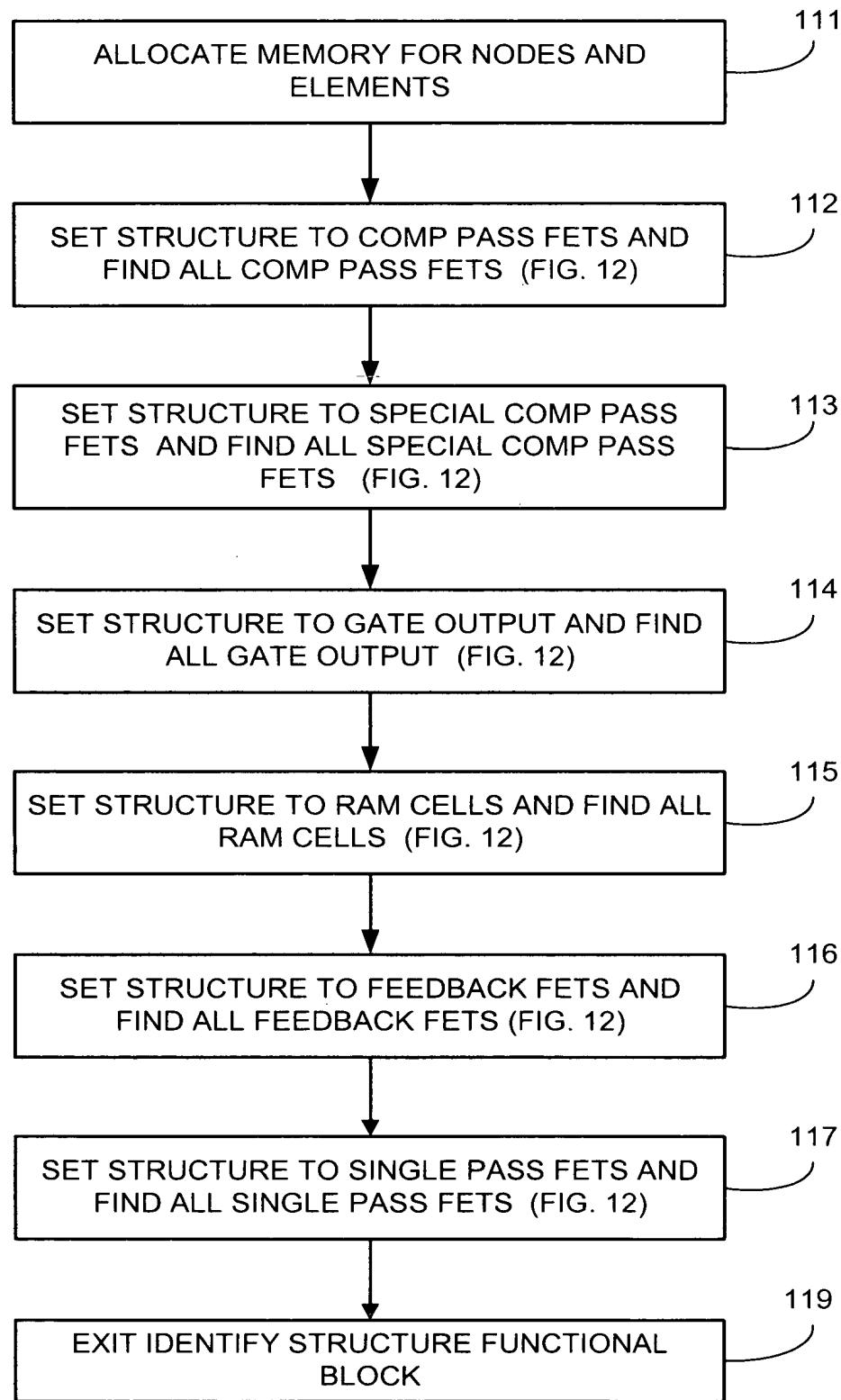
**FIG. 10A**



**FIG. 10B**

**FIG. 11**

110



**FIG. 12**

